



Form 1449 (Modified)	Atty Docket No. ALTRP104/A1212	Application No.: 10/727,781
<b>Information Disclosure Statement By Applicant</b>	Applicant: Gray et al.	
(Use Several Sheets if Necessary)	Filing Date December 3, 2003	Group 2857

#### U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A1						
	A2						
	A3						
	A4						
	A5						

#### Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	B1							
	B2							
	B3							
	B4							
	B5							

#### Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
BPB	C1	Tehrani pour et al., "Embedded Test for Processor and Memory Cores in System-on-Chips", VLSI Circuits and Systems Laboratory, Dept of ECE, The University of Tehran," September 2003
BPB	C2	Campenhout et al., "High-Level Test Generation for Design Verification of Pipelined Microprocessors", ACM 1-58113-109-7/99/06, 1999
	C3	
Examiner	Date Considered	
Bruce P. Borge	6/14/07	

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.